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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of
Jae-Bon KOO, et al.

Docket No. 6161.0077.US

Serial No.: 10/694,941

Group Art Unit: 2879

Filed: October 29, 2003

Examiner: Unassigned

For: **FLAT PANEL DISPLAY AND FABRICATION METHOD THEREOF**

Commissioner for Patents and Trademarks
Washington, D.C. 20231

PETITION FOR ACCELERATED EXAMINATION UNDER 37 C.F.R. 1.102(d)

Sir:

Applicant herein respectfully petitions under 37 CFR §1.102(d) and in accordance with MPEP §708.02 VIII for the accelerated examination of the above-identified application. Applicant attaches a check in the amount of $130.00 as set forth in 37 CFR §1.17(i).

MPEP §708.02 VIII

Applicant is of the opinion that all claims are directed to a single invention. Nevertheless several embodiments of the present invention are disclosed within the application. If required, Applicant requests that the Examiner contact the undersigned for a telephonic election or restriction in accordance with restriction practice to expedite any such issues that may arise.

A pre-examination search was conducted in the U.S. Patent Office. This search included the following classes/subclasses:

Class 257/subclasses 56, 66, 83, 98, 103 and 351

Class 438/subclass 149, 166 and 197

The disclosed references deemed most closely related to the subject matter encompassed by the claims of the above application are discussed below. Attached is an Information Disclosure Statement and PTO Form 1449 prepared in accordance with 37 CFR §1.197 and 1.98 and filed concurrently herewith. The following is a detailed discussion of the references deemed most closely related to the claimed subject matter of the above-identified application, and distinguishing features according to the opinion of the Applicant.

U.S. Pat. No. 5,744,824 to Kousai, *et al.*

A liquid crystal display includes a a semiconductor device with two types of thin film trasnsistors. The two types of thin film transistors have two different property types. One silicon layer is formed and is suitable for a thin film transistor with a relatively large "off" current and a high mobility. Another silicon layer is formed and is suitable for a thin film transistor with a relatively low "off" current and a low mobility.

Applicants respectfully asserts that this patent does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this patent does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. No. 6,548,331 to Lee, *et al.*

A thin film transistor includes a silicon active layer crystallized by a crystallization inducing metal. The crystallization inducing metal is off-set from a channel region of the active layer.

Applicants respectfully asserts that this patent does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this patent does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. No. 6,596,573 to Lee, *et al.*

A thin film transistor includes a polycrystalline active layer. An amorphous silicon layer is located on a substrate by a metal induced lateral crystallization (MILC). A thermal treatment causes the MILC active layer to propogate from the source and drain regions through the contact holes of the thin film transistor.

Applicants respectfully asserts that this patent does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this patent does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. No. 6,639,249 to Valliath

A lighting device with lighting components includes high quality epitaxial layers of monocrystalline materials grown overlaying a monocrystalline silicon.

Applicants respectfully asserts that this patent does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this patent does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. No. 6,692,996 to Lee, *et al.*

A thin film transistor includes a single-crystalized amorphous silicon layer which results from filtering a single crystal component from the ploy-crystal region being crystallized by metal induced lateral crystallization (MILC). The thin film transistor has improved electrical characteristics of electron mobility and leakage current.

Applicants respectfully asserts that this patent does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this patent does not disclose

or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. No. 6,709,910 to Crowder, *et al.*

Film surface protrusions are reduced in the fabrication of laser induced lateral crystallization (LILAC) films. The films are made thicker and oxidized. The extra thickness is then removed to create the smooth surface.

Applicants respectfully asserts that this patent does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this patent does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. No. 6,727,121 to Joo, *et al.*

A thin film transistor includes a single-crystalized amorphous silicon layer which results from filtering a single crystal component from the ploy-crystal region being crystallized by metal induced lateral crystallization (MILC). The thin film transistor has improved electrical characteristics of electron mobility and leakage current.

Applicants respectfully asserts that this patent does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this patent does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. Pub. No. 2002/0074548 to Lee, *et al.*

A thin film transistor includes a polycrystalline active layer. An amorphous silicon layer is located on a substrate by a metal induced lateral crystallization (MILC). A thermal treatment causes

the MILC active layer to propogate from the source and drain regions through the contact holes of the thin film transistor.

Applicants respectfully asserts that this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. Pub. No. 2002/0139979 to Joo, *et al.*

An amorphous silicon layer is crystallized by implanting boron into the amorphous silicon layer during crystallization.

Applicants respectfully asserts that this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. Pub. No. 2002/0196389 to Koyama

An organic light emitting device comprises a plurality of switching thin film transistors, a plurality of driving thin film transistors and a plurality of power controlling thin film transistors.

Applicants respectfully asserts that this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. Pub. No. 2003/0085401 to Joo, *et al.*

An addressing thin film transistor, a pixel driving thin film transistor and a capcaitor include a crystalline silicon thin film. The components are formed at a pixel region of a thin film transistor panel using a metal induced lateral crystallization (MILC). A driving thin film transistor is formed at the periphery of the thin film transistor panel.

Applicants respectfully asserts that this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. Pub. No. 2003/0094613 to Joo, *et al.*

An addressing thin film transistor, a pixel driving thin film transistor and a capcaitor include a crystalline silicon thin film. The components are formed at a pixel region of a thin film transistor panel using a metal induced lateral crystallization (MILC) and a low-concetration doped region. The on-current charactersitic and off current characteristic required for the pixel region and the peripherial region can be simultaneously satisfied.

Applicants respectfully asserts that this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. Pub. No. 2003/0102473 to Chason, *et al.*

Epitaxial layers of monocrystalline materials are grown by forming a compliant substrate for growing the monocrystalline materials. An amorphous silicon layer separates an accomadating layer from a silicon. The amorphous silicon layer permits the growth of the monocrystalline oxide accomadating buffer layer.

Applicants respectfully asserts that this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. Pub. No. 2003/0113949 to Valliath, *et al.*

Epitaxial layers of monocrystalline materials are grown over a monocrystalline layer of silicon. An amorphous silicon layer separates an accomadating layer from a silicon. The amorphous silicon layer permits the growth of the monocrystalline oxide accomadating buffer layer.

Applicants respectfully asserts that this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. Pub. No. 2003/0143794 to Nakamura, *et al.*

A catalytic metal is used to promote crystallization of a semiconductor thin film having an amorphous structure. Phosphorus is added to crystallized poly-silicon film and the resulting poly-silicon is heat treated.

Applicants respectfully asserts that this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. Pub. No. 2004/0046171 to Lee, *et al.*

An amorphous silicon layer is crystallized using metal induced lateral crystallization (MILC) to provide a poly-silicon active layer in a thin film transistor.

Applicants respectfully asserts that this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. Pub. No. 2004/0110329 to Joo, *et al.*

A thin film transistor is formed by consecutively depositing the metal induced lateral crystallization source metal, the thermal annealing for crystallizing the amorphous silicon and activating the doped impurities and depositing the wiring metal all within one equipment while maintaining a vacuum state.

Applicants respectfully asserts that this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. Pub. No. 2004/0125265 to Koo, *et al.*

A crystallization method for a thin film transistor forms a black matrix layer that absorbs external light. The upper region of the black matrix layer has a catalyst for crystallization.

Applicants respectfully asserts that this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. Pub. No. 2004/0130005 to Guzman, *et al.*

A precursor solution of a polycrystalline material is prepared in a solvant with addition of an organic template. The solution is coated on a subtsrate, and an amorphous silcon is deposited on the coated substrate and heat treated. A laser is then used to crystallize the amorphous silicon and form a polycrystalline silicon coated substrate for a semiconductor device.

Applicants respectfully asserts that this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. Pub. No. 2004/0142582 to Crowder, *et al.*

Film surface protrusions are reduced in the fabrication of laser induced lateral crystallization (LILAC) films. The films are made thicker and oxidized. The extra thickness is then removed to create the smooth surface.

Applicants respectfully asserts that this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

U.S. Pat. Pub. No. 2004/0144988 to Jung, *et al.*

An active matrix display device includes a plurality of pixels, with each pixel having at least one thin film transistor. The polycrystalline layer in the device has grain boundaries of substantially identical numbers, substantially identical directions, and occurring at substantially regular intervals.

Applicants respectfully asserts that this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

JP1993-232506

A forward stagger type polycrystalline thin film transistor is used as a driving thin film transistor in a liquid crystal display. A reverse stagger type amorphous thin film transistor is used as the picture element thin film transistor. The polycristalline thin film transistor and the amorphous thin film transistor can be formed on the same substrate.

Applicants respectfully asserts that this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this publication does not disclose or suggest, in combination, at least a first and second transistor, where the

semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

JP2001-202034

An organic electroluminescent (EL) display device has a plurality of thin film transisters and a plurality of organic EL elements. One of the thin film transistors is a P-channel type thin film transistor or an N-channel type thin film transistor.

Applicants respectfully asserts that this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different mobility than the semiconductor layer of the second transistor. Further, this publication does not disclose or suggest, in combination, at least a first and second transistor, where the semiconductor layer in the first transistor has a different crystal structure than the semiconductor layer of the second transistor.

Conclusion

Applicant submits that his present invention is patentable over the above references for at least the reasons discussed herein. Accordingly it is respectfully submitted that this petition be allowed and the present application be designated for accelerated examination. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 23-1951.

Respectfully submitted,

Hae-Chan Park
Registration No. 50,114

November 1, 2004
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Docket No.: 6161.0077.US
Jae-Bon KOO, et al.	
	Group Art Unit: 2879
Appl. No. 10/694,941	Examiner: *To Be Assigned*
Filed: October 29, 2003	
For: **FLAT PANEL DISPLAY AND FABRICATION METHOD THEREOF**	

Information Disclosure Statement

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure under 37 C.F.R. §§ 1.56, 1.97 and 1.98, applicant respectfully brings the following information listed on accompanying Form PTO-1449 to the attention of the examiner.

Where the publication date of a listed document does not provide a month of publication, the year of publication of the listed document is sufficiently earlier than the effective U.S. filing date and any foreign priority date so that the month of publication is not in issue. Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be

prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith. It is further understood that the Examiner will consider information that had been cited by or submitted to the U.S. Patent and Trademark Office in a prior application relied on under 35 U.S.C. §120. 1138 OG 37, 38 (May 19, 1992).

Applicants have checked the appropriate boxes below.

☒ 1. This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits OR before the mailing date of a first Office Action after the filing of a request for continued examination under 37 C.F.R. §1.114. No certification or fee is required.

☐ 2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection or Notice of Allowance.

☐ a. I hereby certify that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. Attached is our Check No. _____ in the amount of $ _____ in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 3. This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. It is hereby requested that the Information Disclosure Statement be considered. Attached is our Check No. _____ in the amount of $ _____ in payment of the fee under 37 C.F.R. § 1.17(i)(1).

☐ a. I hereby certify that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 4. Relevance of the non-English language document(s) is discussed in the present specification.

☐ 5. The document(s) was/were cited in a corresponding foreign application. An English language version of the foreign search report is attached for the Examiner's information.

☐ 6. A concise explanation of the relevance of the non-English language document(s) appears below:

☐ 7. The Examiner's attention is directed to co-pending U.S. Patent Application No. _____, filed _____, which is directed to related technical subject matter. The identification of this U.S. Patent Application is not to be construed as a waiver of secrecy as to that application now or upon issuance of the present application as a patent. The Examiner is respectfully requested to

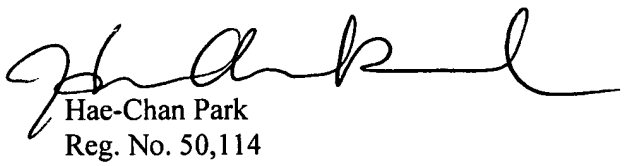
consider the cited application and the art cited therein during examination.

☐ 8. Copies of the documents were cited by or submitted to the Office in Application No. _____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449, and to indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 23-1951.

Respectfully submitted,



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Date: November 1, 2004

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Form PTO-1449 (Modified)	Attorney Docket No.: 6161.0077.US	Serial No.: 10/694,941
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	Applicant: Jae-Bon KOO, *et al.*	
(Use several sheets if necessary) Page 1 of 1	Filing Date: October 29, 2003	Group: 2879

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINERS INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
		5,744,824	Apr. 24, 1998	Kousai et al.			
		6,548,331 B2	Apr. 15, 2003	Lee et al.			
		6,596,573 B2	Jul. 22, 2003	Lee et al.			
		6,639,249 B2	Oct. 28, 2003	Valliath			
		6,692,996 B2	Feb. 17, 2004	Lee et al.			
		6,709,910 B1	Mar. 23, 2004	Crowder et al.			
		6,727,121	Apr. 27, 2004	Jou et al.			
		2002/0074548 A1	Jun. 20, 2002	Lee et al.			
		2002/0139979 A1	Oct. 3, 2002	Joo et al.			
		2002/0196389 A1	Dec. 26, 2002	Koyama			
		2003/0085401 A1	May 8, 2003	Joo et al.			
		2003/0094613 A1	May 22, 2003	Joo et al.			
		2003/0102473 A1	Jun. 5, 2003	Chason et al.			
		2003/0113949 A1	Jun. 19, 2003	Valliath			
		2003/0143794 A1	Jul. 31, 2003	Nakamura et al.			
		2004/0046171 A1	Mar. 11, 2004	Lee et al.			
		2004/0110329 A1	Jun. 10, 2004	Joo et al.			
		2004/0125265 A1	Jul. 1, 2004	Koo et al.			
		2004/0130005 A1	Jul. 8, 2004	Guzman et al.			
		2004/0142582 A1	Jul. 22, 2004	Crowder et al.			
		2004/0144988 A1	Jul. 29, 2004	Jung			
		2004/0169182 A1	Sep. 2, 2004	Koo et al.			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
		Abstract of JP5232506	Sep. 10, 1993	Japan			☒ Abstract	
		Abstract of JP2001202034	Jul. 27, 2001	Japan			☒ Abstract	
							☐	
							☐	

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicant.